

**THE KAVERY ENGINEERING COLLEGE***(An Autonomous Institution)***B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025***Third Semester**Computer Science and Engineering***CS3351- Digital Principles and Computer Organization****(Common to Information Technology & Artificial Intelligence and Data Science)***Regulations - 2021**Duration : 3 Hrs**Maximum : 100 Marks***PART - A (ANSWER ALL QUESTIONS) (Marks 10\*2=20)**

| <i>Q.No</i> | <i>Questions</i>                                         | <i>BTL</i> | <i>CO</i> | <i>Marks</i> |
|-------------|----------------------------------------------------------|------------|-----------|--------------|
| 1.          | Outline the logic circuit of half subtractor.            | L2         | 1         | 2            |
| 2.          | Compare the function of decoder and encoder.             | L4         | 1         | 2            |
| 3.          | Differentiate Synchronous and Asynchronous Counter.      | L2         | 2         | 2            |
| 4.          | Define State Table.                                      | L1         | 2         | 2            |
| 5.          | Define instruction set architecture.                     | L1         | 3         | 2            |
| 6.          | List the relative addressing mode with an example.       | L1         | 3         | 2            |
| 7.          | Differentiate Static and Dynamic branch prediction.      | L2         | 4         | 2            |
| 8.          | Outline the concept of a data hazard.                    | L2         | 4         | 2            |
| 9.          | Define memory management.                                | L1         | 5         | 2            |
| 10.         | Classify the three types of the DMA transfer techniques. | L1         | 5         | 2            |

**PART - B (ANSWER ALL QUESTIONS) (Marks 5\*16 = 80)**

| <i>Q.No</i> | <i>Questions</i>                                                                                                                                                                                                                                                                               | <i>BLT</i> | <i>CO</i> | <i>Marks</i> |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----------|--------------|
| 11.         | a Solve the following function using Karnaugh Map:<br>i. $F(A,B,C,D)=\Sigma(0,1,2,4,5,6,8,9,12,13,14)$<br>ii. $F(w,x,y,z) = \Sigma (1,3,7,11,15) + d(0,2,5)$<br>Or<br>b Apply the multiplexer and Simplify the following function using 8x1 Mux F<br>(A, B, C, D) = $\Sigma(0,1,3,4,8,9,15)$ . | L3         | 1         | 16           |
| 12.         | a Analyze the working of SR, JK, D, and T flip-flops. Draw the operation and excitation tables for each flip-flop with logic diagrams.<br>Or<br>b Examine the different types of shift registers with neat diagram.                                                                            | L4         | 2         | 16           |
| 13.         | a i Illustrate about ISA with relevant diagrams.<br>ii Illustrate the von Newmann architecture with neat diagram.<br>Or<br>b Explain the different types of addressing modes with an example.                                                                                                  | L2         | 3         | 8            |
|             |                                                                                                                                                                                                                                                                                                | L2         | 3         | 8            |
|             |                                                                                                                                                                                                                                                                                                | L2         | 3         | 16           |

|     |   |                                                                                                                                     |    |   |    |
|-----|---|-------------------------------------------------------------------------------------------------------------------------------------|----|---|----|
| 14. | a | Classify the different types of data paths used in computer architecture and discuss their respective advantages and disadvantages. | L4 | 4 | 16 |
|     |   | Or                                                                                                                                  |    |   |    |
|     | b | Examine a 4 stage Instruction Pipeline. Explain the issues affecting Pipeline performance.                                          | L4 | 4 | 16 |
| 15. | a | Explain how virtual memory management supports multitasking in operating systems. Give one practical example.                       | L2 | 5 | 16 |
|     |   | Or                                                                                                                                  |    |   |    |
|     | b | Explain the importance of DMA in reducing CPU workload during data transfers. Provide an example.                                   | L2 | 5 | 16 |